What is claimed is:

1. A high voltage device comprising:
a substrate of a first type;
a first and second well respectively of the first and a second type in the substrate;
a gate formed on the substrate;
a first and second doped region both of the second type, respectively formed in the first and second well and both sides of the gate; and
a third doped region of the first type in the first well and adjacent to the first doped region.

2. The high voltage device as claimed in claim 1 further comprising field oxides isolating the high voltage device from other devices on the substrate.

3. The high voltage device as claimed in claim 1, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.

4. The high voltage device as claimed in claim 3 further comprising a fourth lightly doped region of the second type adjacent to the first doped region and beneath one of the spacers.

5. The high voltage device as claimed in claim 1, wherein there is a spacing of the second doped region to the gate.

6. The high voltage device as claimed in claim 1, wherein the overlay of the gate and the second well is defined as zero.

7. The high voltage device as claimed in claim 1, wherein the first and second types are respectively P and N type.

8. The high voltage device as claimed in claim 1, wherein the first and second type are respectively N and P type and the high voltage device further comprises a N+ buried layer in the substrate and beneath the first and second well.

9. A high voltage device formed on a P substrate comprising:

an HVNMOS comprising:

a first P and N well in the P substrate;

a first gate formed on the P substrate;

two first N+ doped regions respectively formed in the first P and N well, and both sides of the first gate; and

a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and

a HVPMOS comprising:

an N+ buried layer in the P substrate;

a second N and P well in the P substrate and above the N+ buried layer;

a second gate formed on the P substrate;

two second P+ doped regions respectively formed in the second N and P well, and both sides of the second gate; and

a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

10. The high voltage device as claimed in claim 9 further comprising field oxides isolating the HVPMOS and HVNMOS from other devices on the P substrate.

11. The high voltage device as claimed in claim 9, wherein each of the first and second gates comprise a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

12. The high voltage device as claimed in claim 11, wherein the HVNMOS further comprises an N lightly doped region adjacent to the first N doped region in the first P well and beneath one of the spacers of the first gate, and the HVPMOS further comprises a P lightly doped region adjacent to the second P doped region in the second N well and beneath one of the spacers of the second gate.

13. The high voltage device as claimed in claim 9, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

14. The high voltage device as claimed in claim 9, wherein the overlay of the first gate and the first P well,

and the second gate and the second N well are defined as zero.

15. A method for manufacturing a high voltage device, comprising the steps of:

providing a substrate of a first type;

forming a first and second well respectively of the first and a second type in the substrate;

forming a gate on the substrate;

forming a first and second doped region both of the second type, respectively in the first and second well and both sides of the gate; and

forming a third doped region of the first type in the first well and adjacent to the first doped region.

16. The method as claimed in claim 15 further comprising the step of:

forming field oxides isolating the high voltage device from other devices on the substrate.

17. The method as claimed in claim 15, wherein the gate comprises a gate oxide on the substrate, a conducting layer on the gate oxide and spacers on two sides of the gate oxide and conducting layer.

18. The method as claimed in claim '17 further comprising the step of:

forming a fourth lightly doped region of the second type adjacent to the first doped region and beneath one of the spacers.

19. The method as claimed in claim 15, wherein there is a spacing of the second doped region to the gate.

20. The method as claimed in claim 15, wherein the overlay of the gate and the second well is defined as zero.

21. The method as claimed in claim 15, wherein the first and second type are respectively P and N type.

22. The method as claimed in claim 1, wherein the first and second type are respectively N and P type and the method further comprises the step of:

forming an N+ buried layer in the substrate and beneath the first and second well.

23. A method for manufacturing a high voltage device comprising the steps of:

providing a P substrate;

forming a HVNMOS on the P substrate by:

forming a first P and N well in the P substrate;

forming a first gate on the P substrate;

forming two first N+ doped regions respectively in the first P and N well, and both sides of the first gate; and

forming a first P+ doped region in the first P well and adjacent to the first N+ doped region in the first P well; and

forming a HVPMOS on the P substrate by:

forming an N+ buried layer in the P substrate;

forming a second N and P well in the P substrate and above the N+ buried layer;

forming a second gate on the P substrate;
forming two second P+ doped regions respectively in the second N and P well, and both sides of the second gate; and
forming a second N+ doped region in the second N well and adjacent to the second P+ doped region in the second N well.

24. The method as claimed in claim 23 further comprising the step of:
forming field oxides isolating the HVPMOS and HVNMOS from other devices on the P substrate.

25. The method as claimed in claim 23, wherein each of the first and second gate comprises a gate oxide on the P substrate, a conducting layer on the gate oxide and spacers on both sides of the gate oxide and conducting layer.

26. The method as claimed in claim 25 further comprising the steps of:
forming a N lightly doped region adjacent to the first N doped region in the first P well and beneath one of the spacers of the first gate; and
forming a P lightly doped region adjacent to the second P doped region in the second N well and beneath one of the spacers of the second gate.

27. The method as claimed in claim 23, wherein there is spacing of the first N+ doped region in the first N well to the first gate and the second P+ doped region in the second P well to the second gate.

28. The method as claimed in claim 23, wherein the overlay of the first gate and the first P well, and the second gate and the second N well are defined as zero.